

4410/4412 DDS Urukul

Features

- 4-channel 1GS/s DDS
- Output frequency from <1 to >400 MHz
- Sub-Hz frequency resolution
- Controlled phase steps
- Accurate output amplitude control

Applications

- Dynamic low-noise RF source
- Driving RF electrodes in ion traps
- Driving acousto-optic modulators
- Form a laser intensity servo with 5108 Sampler

General Description

The 4410/4412 DDS Urukul card is a 4hp Sinara EEM, part of the ARTIQ/Sinara family. It adds frequency generation capabilities to carrier cards such as 1124 Kasli and 1125 Kasli-SoC. It can also be combined with 5018 ADC Sampler to form the ARTIQ SU-Servo configuration.

It provides 4 channels of DDS (direct digital synthesis) at 1GS/s. Output frequencies from <1 to >400 MHz are supported. The nominal maximum output power of each channel is 10dBm. Each channel can be attenuated from 0 to -31.5 dB by a digital attenuator. RF switches (1ns temporal resolution) on each channel provide 70 dB isolation.

4410 DDS Urukul features AD9910 chips, while 4412 DDS Urukul features AD9912 chips. These offer slightly different features and specifications. See below for a comparison between the two.

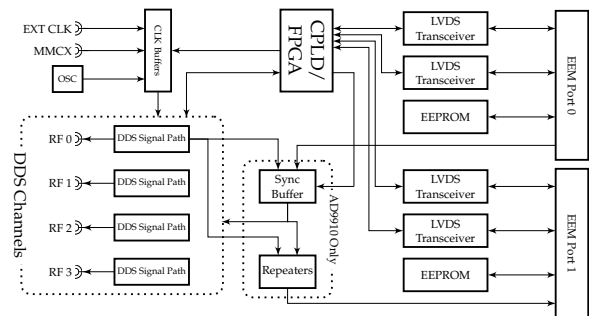


Figure 1: Simplified Block Diagram

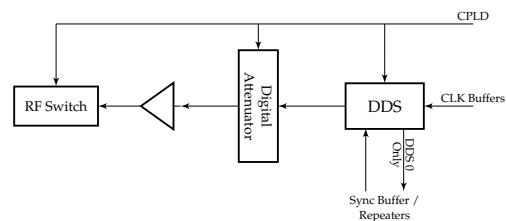


Figure 2: Simplified DDS Signal Path

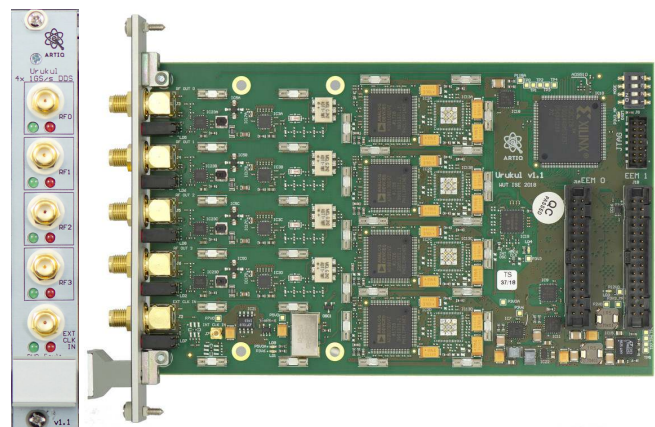


Figure 3: Urukul card and front panel

Source

4410/4412 DDS Urukul, like all the Sinara hardware family, is open-source hardware, and design files (schematics, PCB layouts, BOMs) can be found in detail at the repository <https://github.com/sinara-hw/Urukul/>.

Model comparison

4410 DDS Urukul uses AD9910¹ chips, whereas 4412 DDS Urukul uses AD9912² chips. In general, 4412/AD9912 is capable of much higher frequency resolution, at the cost of more detailed control features provided by 4410/AD9910, such as phase synchronization, digital ramp modulation or DRG, and digital amplitude control. See individual DDS IC datasheets for feature details, especially of AD9910, or ARTIQ code section below for examples of more complex experiments only possible with AD9910. The SUServo configuration is only available for AD9910.

Table 1: Specification Differences

Parameter	AD9910	AD9912	Unit	Conditions
Resolution				
Frequency ^{1,5}	0.25		Hz	
		8	μHz	
Phase offset ^{1,2}	16	14	bits	
DAC full scale current ^{1,2}	8	10	bits	
Digital amplitude ¹	14		bits	
Power consumption ⁵	7	6.5	W	4x 400 MHz, 10.5 dBm, 52°C
ARTIQ SUServo available	Yes	No		

Electrical Specifications

Specifications of parameters are based on the datasheets of the DDS IC (AD9910¹, AD9912AD9912²), clock buffer IC (Si53312³), digital attenuator IC (HMC542BLP4E⁴), Sinara project information⁵ and corresponding test results⁶.

Table 2: Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Unit	Conditions
Clock input					
Input frequency ^{1,2}	10		1000	MHz	PLL disabled
	3.2		60	MHz	AD9910, PLL enabled, no clock division
	12.8		240	MHz	AD9910, PLL enabled, 4x clock division
	11		200	MHz	AD9912, PLL enabled, no clock division
	44		800	MHz	AD9912, PLL enabled, 4x clock division

¹<https://www.analog.com/media/en/technical-documentation/data-sheets/AD9910.pdf>

²<https://www.analog.com/media/en/technical-documentation/data-sheets/AD9912.pdf>

³https://www.skyworksinc.com/-/media/SkyWorks/SL/documents/public/data-sheets/Si5331x_datasheet.pdf

⁴<https://www.analog.com/media/en/technical-documentation/data-sheets/hmc542b.pdf>

⁵<https://github.com/sinara-hw/Urukul/wiki#details-specification-and-typical-performance-data>

⁶<https://github.com/sinara-hw/sinara/issues/354#issuecomment-352859041>

Table 3: Recommended Operating Conditions, cont.

Parameter	Min.	Typ.	Max.	Unit	Conditions
Nominal input power ³		10		dBm	

Table 4: RF Output Specifications

Parameter	Min.	Typ.	Max.	Unit	Conditions
Low frequency power ⁶			-20	dBm	100 kHz output
			10	dBm	1 MHz output
Frequency ⁵	1		400	MHz	
Digital attenuation ⁴	-31.5		0	dB	
Resolution					
Temporal (I/O Update) ⁵		4		ns	
Digital attenuation ⁴		0.5		dB	
Fixed pre-amplification ⁷		23		dB	
Fixed attenuation ⁷		9		dB	

Table 5: Electrical Characteristics

Parameter	Min.	Typ.	Max.	Unit	Conditions
Digital attenuator glitch duration ⁶		100		ns	
RF switch ⁶					
Rise to 90%		100		ns	
Isolation		70		dB	
Turn-on chirp			0.1	deg/s	Excluding the first μ s
Crosstalk ⁶		-84		dB	Victim RF switch opened
		-110		dB	Victim RF switch closed
Cross-channel-intermodulation ⁶		-90		dB	

⁷ Users should note that the relatively high onboard amplification of the ERA3-SM+ can result in clipping with high output power if the digital attenuator is not used. <https://github.com/sinara-hw/Urukul/issues/39>

Table 6: Electrical Characteristics, cont.

Parameter	Min.	Typ.	Max.	Unit	Conditions
Phase noise ⁶		-85		dBc/Hz	0.1 Hz
		-95		dBc/Hz	1 Hz
		-107		dBc/Hz	10 Hz
		-116		dBc/Hz	100 Hz
		-126		dBc/Hz	1 kHz
		-133		dBc/Hz	10 kHz
		-135		dBc/Hz	100 kHz
		-128		dBc/Hz	1 MHz
		-149		dBc/Hz	10 MHz
Second-order harmonics ⁶		-40		dB	6 dBm output
		-34		dB	10.5 dBm output
Third-order harmonics ⁶		-54		dB	6 dBm output
		-28		dB	10.5 dBm output

The tabulated performance characteristics above were produced using the following setup unless otherwise noted:

- 100 MHz input clock into SMA, 10 dBm
- Input clock divided by 4
- PLL with x40 multiplier
- Output frequency at 80 MHz or 81 MHz

Harmonic content

Harmonic content of the DDS signals from 4410 DDS Urukul is tabulated below⁸. An external 125 MHz clock signal was supplied.

Table 7: Harmonic content with 0.0 dB digital attenuation

Frequency (MHz)	Output power (dBm) of the n th -order harmonic								
	1 st	2 nd	3 rd	4 th	5 th	6 th	7 th	8 th	9 th
0.1	-21.14	-59.03	-54.93	-93.07	-73.38	-94.07	-84.78	-91.77	-96.61
0.5	4.51	-15.45	-11.61	-25.02	-24.35	-51.70	-35.14	-34.46	-37.85
1	7.67	-16.80	-12.32	-18.27	-29.25	-30.87	-34.51	-39.28	-39.84
10	10.67	-12.69	-13.94	-26.12	-27.76	-36.11	-55.32	-43.85	-42.65
20	10.86	-24.90	-13.65	-22.87	-28.67	-47.68	-35.85	-35.45	-38.48
50	10.74	-14.18	-15.01	-27.57	-29.01	-38.05	-51.52	-44.53	-42.71
100	9.70	-33.59	-16.72	-34.36	-26.81	-40.14	-41.07	-43.88	-56.89
200	8.97	-22.22	-16.23	-24.89	-30.49	-37.97	-37.79	-38.80	-40.14
300	8.27	-19.17	-19.51	-29.80	-34.75	-38.90	-51.92	-53.38	-57.95
400	7.68	-17.82	-21.60	-33.04	-37.80	-50.37	-57.45	-59.80	-64.68
500	-1.80	-41.57	-51.71	-72.36	-89.35	-91.63	-93.15	-84.54	-107.57

Table 8: Harmonic content with 10.0 dB digital attenuation

Frequency (MHz)	Output power (dBm) of the n th -order harmonic								
	1 st	2 nd	3 rd	4 th	5 th	6 th	7 th	8 th	9 th
0.1	-27.06	-81.35	-62.09	-97.37	-84.11	-103.78	-91.37	-100.48	-104.22
0.5	-3.2	-37.82	-52.21	-66.76	-77.86	-85.92	-86.37	-97.59	-120.76
1	-0.43	-34.47	-47.80	-75.28	-86.45	-101.91	-93.22	-96.14	-106.71
10	1.95	-31.04	-28.23	-51.76	-57.29	-76.26	-78.15	-83.85	-80.20
20	2.10	-33.05	-28.30	-54.50	-52.31	-72.39	-70.96	-82.98	-82.58
50	1.89	-33.24	-28.50	-52.67	-48.35	-74.77	-77.26	-79.33	-73.58
100	0.80	-38.51	-63.22	-61.73	-71.97	-97.45	-97.67	-107.40	-93.03
200	0.05	-38.25	-42.16	-63.01	-84.55	-82.66	-108.85	-116.62	-99.45
300	-0.51	-35.91	-48.83	-82.43	-100.53	-111.79	-118.62	-120.05	-97.72
400	-1.20	-38.37	-49.77	-89.45	-74.66	-108.12	-116.75	-114.08	-102.29
500	-11.20	-61.47	-77.59	-74.73	-100.23	-93.12	-99.83	-86.71	-112.63

⁸<https://github.com/sinara-hw/Urukul/issues/29>

Table 9: Harmonic content with 20.0 dB digital attenuation

Frequency (MHz)	Output power (dBm) of the n th -order harmonic								
	1 st	2 nd	3 rd	4 th	5 th	6 th	7 th	8 th	9 th
0.1	-31.06	-82.29	-68.34	-109.04	-92.48	-111.23	-99.94	-109.85	-112.36
0.5	-11.99	-56.69	-71.73	-95.76	-101.86	-114.37	-102.81	-106.94	-116.72
1	-9.94	-54.54	-56.49	-89.12	-105.94	-110.93	-102.79	-107.01	-117.29
10	-7.89	-50.19	-57.35	-91.36	-97.88	-107.95	-103.53	-96.04	-108.26
20	-7.79	-52.72	-58.03	-90.75	-99.82	-102.07	-101.55	-104.73	-103.31
50	-7.96	-52.36	-59.26	-84.44	-87.55	-86.88	-97.76	-92.61	-83.19
100	-9.04	-57.40	-61.76	-78.50	-91.80	-117.64	-107.40	-112.64	-102.07
200	-9.73	-57.39	-72.31	-72.66	-93.26	-95.95	-125.22	-122.35	-130.24
300	-10.27	-58.65	-74.60	-109.24	-107.74	-115.75	-125.36	-124.54	-98.86
400	-10.94	-59.62	-79.36	-98.48	-74.72	-111.95	-119.18	-114.63	-104.34
500	-21.00	-78.52	-99.07	-74.91	-99.55	-92.91	-103.02	-87.33	-114.87

Table 10: Harmonic content with 31.5 dB digital attenuation

Frequency (MHz)	Output power (dBm) of the n th -order harmonic								
	1 st	2 nd	3 rd	4 th	5 th	6 th	7 th	8 th	9 th
0.1	-37.89	-85.04	-77.41	-122.04	-114.29	-115.58	-110.65	-120.06	-123.70
0.5	-22.38	-71.24	-89.84	-107.81	-108.76	-127.83	-114.12	-118.34	-127.07
1	-21.01	-72.10	-90.08	-111.97	-111.30	-127.43	-114.38	-118.07	-128.06
10	-19.22	-72.13	-90.74	-110.14	-105.28	-114.04	-113.51	-94.85	-116.15
20	-19.28	-75.95	-94.72	-91.71	-107.55	-112.85	-112.24	-116.33	-114.02
50	-19.27	-74.93	-92.21	-95.77	-101.06	-97.92	-108.30	-103.60	-93.96
100	-20.27	-79.05	-87.48	-89.73	-104.00	-117.98	-112.12	-110.51	-105.80
200	-21.19	-78.33	-106.81	-82.70	-92.31	-109.93	-133.86	-120.94	-102.95
300	-21.58	-80.96	-112.44	-110.40	-108.11	-115.68	-122.51	-125.25	-99.63
400	-22.44	-82.73	-105.55	-98.03	-74.84	-113.93	-119.41	-114.93	-104.55
500	-31.73	-93.37	-99.74	-75.03	-99.27	-92.84	-104.14	-87.46	-116.22

RMS voltage

The RMS voltage of a 4410 DDS Urukul channel at different amplitude scale factors is measured below. The DDS channel is directly connected to an oscilloscope with a 50Ω~termination. The reported values are obtained from the oscilloscope.

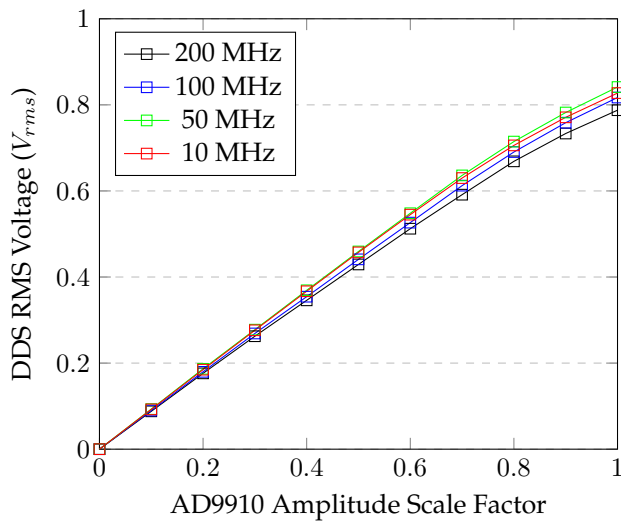


Figure 4: RMS voltage, 0dB attenuation

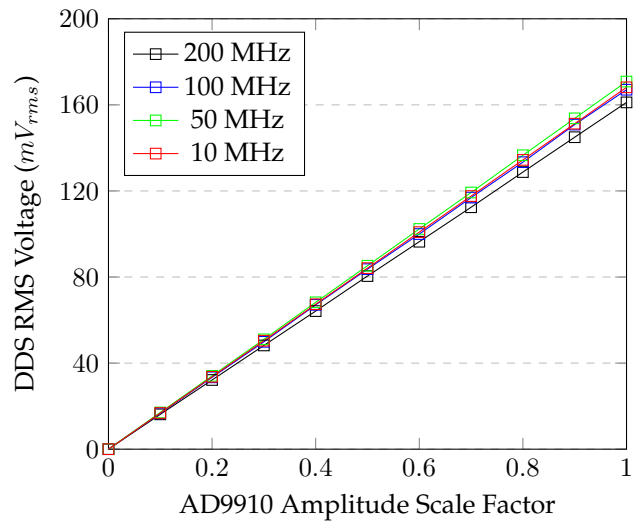


Figure 5: RMS voltage, 15dB attenuation

The ideal RMS voltage is described by the linear function $V_{rms,ideal}(ASF) = \frac{V_{rms}(0.1)}{0.1} * ASF$. The measured RMS voltage divided by the full scale ideal RMS voltage (i.e. $V_{rms,ideal}(1)$) is shown below.

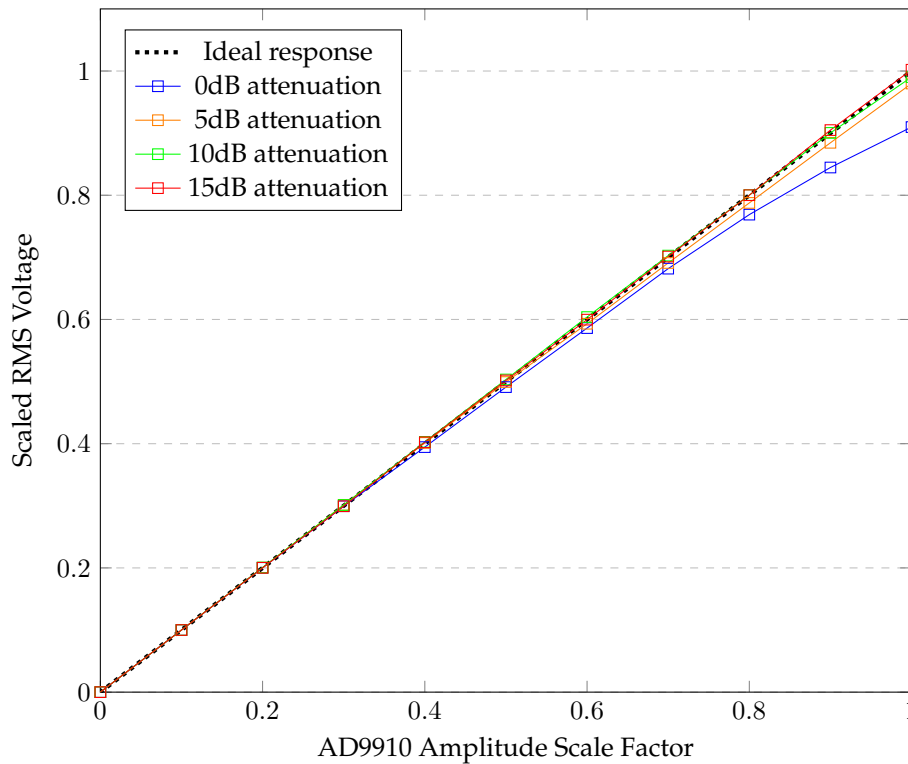


Figure 6: RMS voltage scaled by ideal voltage at ASF=1, 100 MHz

Further graphical data

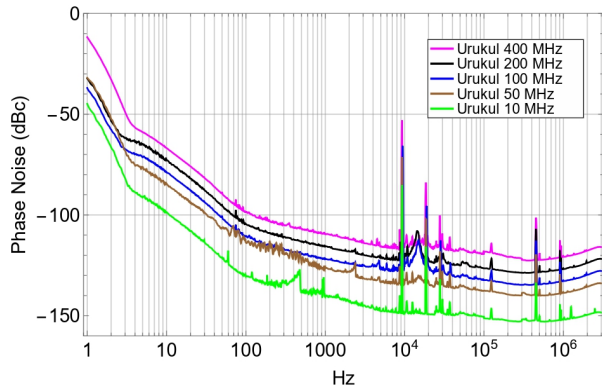


Figure 7: Phase noise of Urukul clocked by internal oscillator

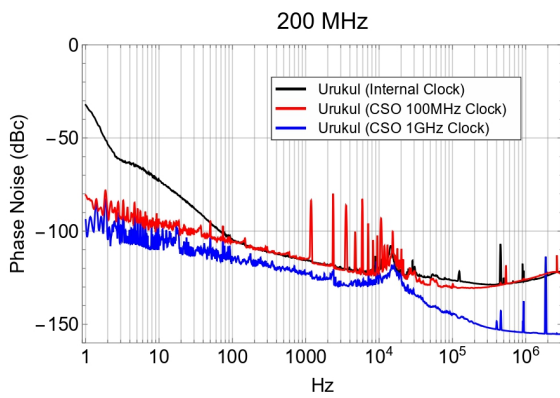


Figure 8: Phase noise of 200 MHz DDS Output

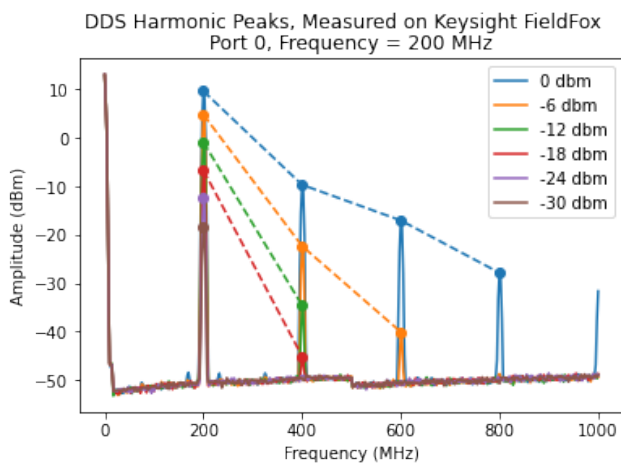


Figure 9: Harmonic content of 200 MHz DDS Output⁹

⁹<https://github.com/sinara-hw/Urukul/issues/64>

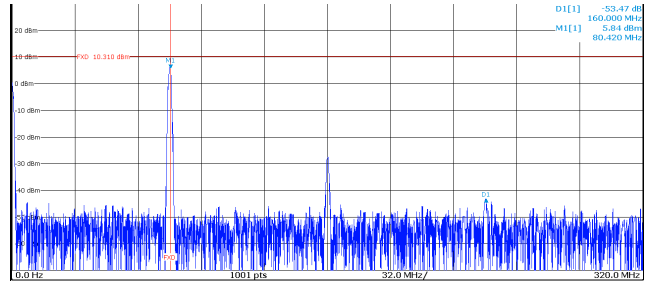


Figure 10: Harmonic content of 80 MHz DDS Output (6 dBm)⁶

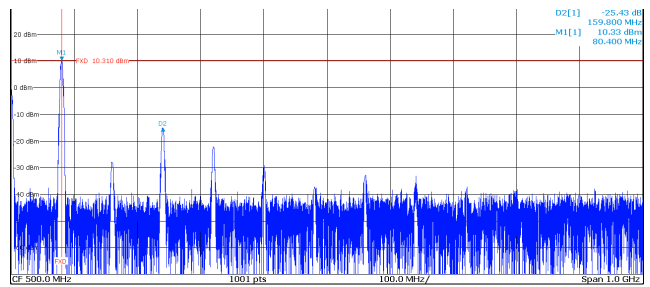


Figure 11: Harmonic content of 80 MHz DDS Output (10 dBm)⁶

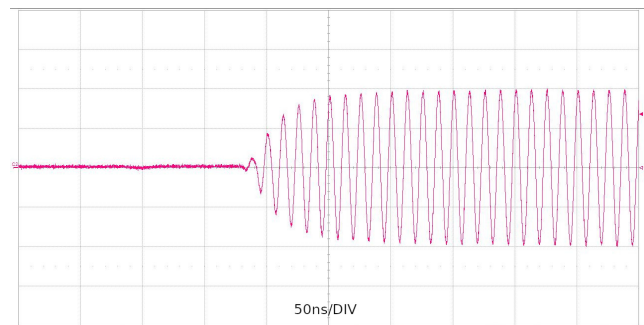


Figure 12: RF switch turn on transient⁶

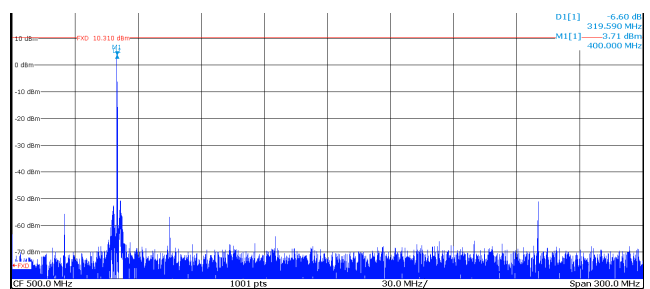


Figure 13: Nyquist rejection 400 MHz to 600 MHz⁶

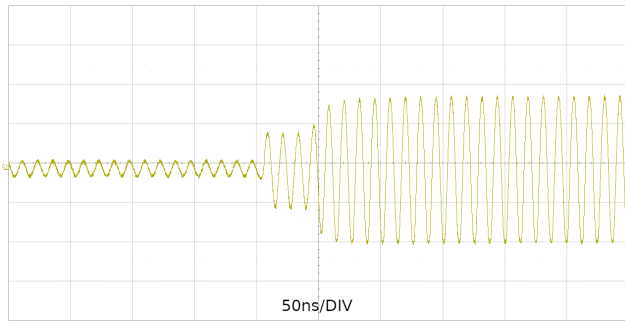


Figure 14: Attenuator step from 20 to 60 digital (16+4dB switch glitch)⁶

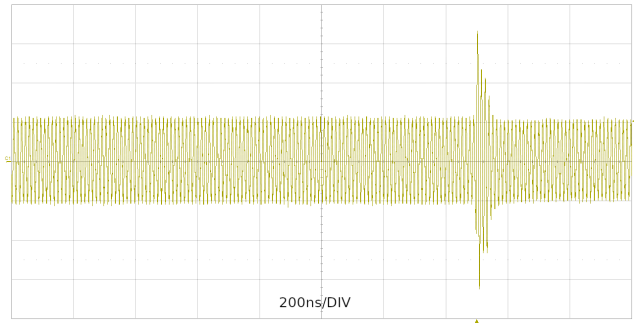


Figure 17: Attenuator step from 31 to 32 digital (major carry glitch)⁶

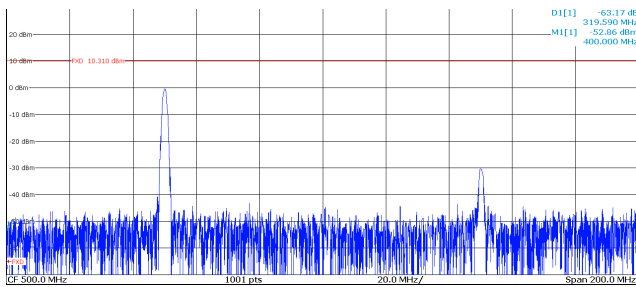


Figure 15: Nyquist rejection 450 MHz to 550 MHz⁶

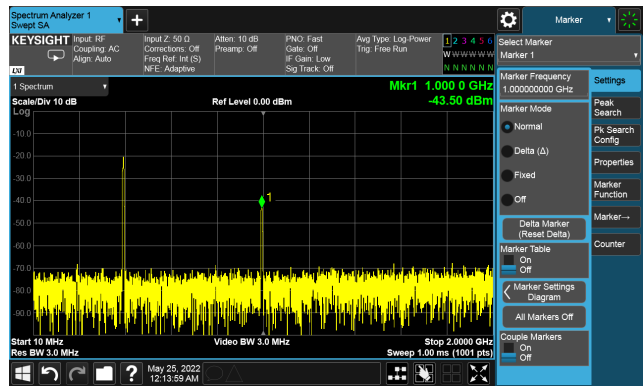


Figure 18: Crosstalk seen with 1 GHz external clock, Urukul 1.5¹⁰

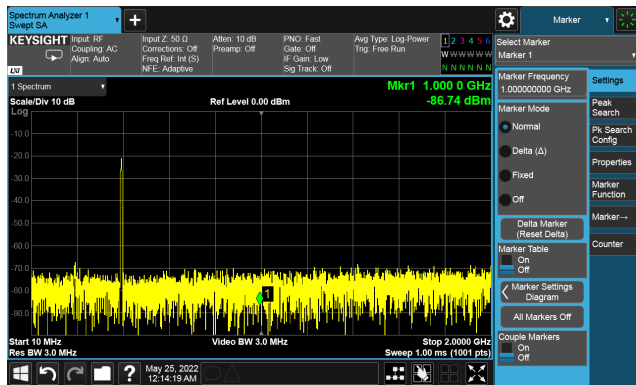


Figure 16: No crosstalk, 1 GHz external clock, Urukul 1.5¹⁰, LPF applied

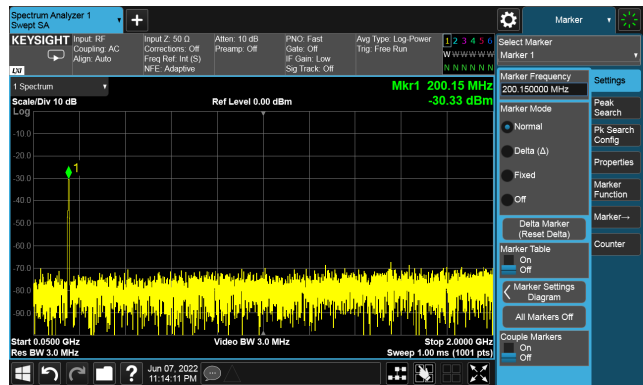


Figure 19: No crosstalk, 1 GHz external clock, Urukul 1.5¹⁰, front panel removed

¹⁰ Issue caused by improperly grounded SMA connectors in front panel, fixed in hardware revisions v1.5.5 and later. See <https://github.com/sinara-hw/Urukul/issues/68>

Front panel LEDs

4410/4412 Urukul features several indicator LEDs on the front panel. Each of the four RF channels has:

- A green LED, which indicates that the RF output is enabled
- A red LED, which:
 - can be turned on by the user¹¹
 - (4410 only) indicates a DDS synchronization/PLL issue¹²

Two additional LEDs indicate power good (green) and overtemperature (red).

Configuring Operation Mode

Modern Urukul revisions

In modern Urukul hardware revisions (v1.6 and later) the CPLD is replaced by an FPGA and mode of operation no longer needs to be specified by DIP switch. It is only necessary to flash the correct gateway. PLD gateway code is open-source and can be found with flashing instructions at <https://git.m-labs.hk/M-Labs/urukul-pld>.

Urukul v1.5 and earlier

In older Urukul hardware revisions (v1.5 and earlier) mode of operation was specified by a DIP switch. The DIP switch can be found at the top right corner of the card. The following table summarizes the required setting for each mode. ✓ indicates ON, while ✗ indicates OFF.

Table 11: DIP switch configurations

Mode	DIP Switch			
	1	2	3	4
Default	✗	✗	✗	✗
SU-Servo	✓	✓	✗	✗

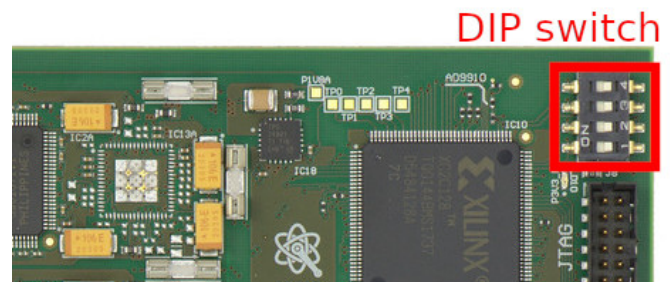


Figure 20: Position of DIP switch

Urukul Single-/Double-EEM Modes

4410/4412 DDS Urukul cards can operate with either a single or double EEM connections. When only EEM0 is connected, the card will act in single-EEM mode; when both EEM0 and EEM1 are connected, the card will act in double-EEM mode.

Double-EEM mode additionally provides 1 ns temporal resolution RF switches. Without EEM1, the only way to access the switches is through the CPLD, using SPI. With EEM1, RF switches can be controlled as a TTL output through the LVDS transceiver. 1 ns temporal resolution can then be achieved using the ARTIQ RTIO system. Double-EEM mode is also recommended for the SUServo configuration.

¹¹See the `led` parameter of `urukul.cfg` in ARTIQ core real-time drivers

¹²The LED may stay on when PLL is bypassed in ARTIQ (see below)

ARTIQ System Description Entry

ARTIQ/Sinara firmware/gateway is generated according to a JSON system description file, allowing gateway to be specific to and optimized for a certain system configuration.

4410/4412 Urukul should be entered in the peripherals list of the corresponding core device in the following format:

```
{
  "type": "urukul",
  "proto_rev": 9, // current CPLD firmware version
  "dds": "ad9910", // or "ad9912", as appropriate
  "ports": [0, 1], // second port is optional
  "synchronization": true, // or false, for AD9910 only
  "clk_sel": 2, // select 0 to 2 for clock source
  "pll_en": 0 // PLL bypass, for higher external frequencies
  "refclk": 125e6, // for external clock signal
}
```

Replace 0 and 1 with the EEM port numbers used on the core device. Any ports can be used. For single-EEM mode, simply specify only one port. The `synchronization` field is boolean, false by default, and only applies to AD9910. In the `clk_sel` field, 0 represents the internal 100 MHz oscillator, 1 represents SMA input, and 2 represents MMCX input. The `pll_en` field may be specified 0 or 1 and is 1 by default.

Note that the SUServo configuration requires a different system description entry. See SUServo section below.

Example ARTIQ Code

The sections below demonstrate simple usage scenarios of extensions on the ARTIQ control system. These extensions make use of the resources of the 4410/4412 DDS Urukul. They do not exhaustively demonstrate all the features of the ARTIQ system.

The full documentation for ARTIQ software and gateway, including guides for their use, is available at <https://m-labs.hk/artiq/manual/>. Please consult the manual for details and reference material of the functions and structures used here.

For details of AD9910 capabilities, operation modes, profiles, signals, etc., see also the corresponding datasheet, e.g. <https://www.analog.com/media/en/technical-documentation/data-sheets/AD9910.pdf>.

10 MHz sinusoidal wave

Generates a 10MHz sinusoid from RF0 with full scale amplitude, attenuated by 6 dB. Both the CPLD and the DDS channels should be initialized. By default, AD9910 single-tone profiles are programmed to profile 7.

```
@kernel
def run(self):
    self.core.reset()
    self.urukul0_cpld.init()
    self.urukul0_ch0.init()
    self.urukul0_ch0.cfg_sw(True)
    self.urukul0_ch0.set_att(6.*dB)
    self.urukul0_ch0.set(10*MHz)
```

If the synchronization feature of AD9910 is enabled, RF signal across different channels of the same Urukul can be synchronized. For example, phase-coherent RF signal can be produced on both channel 0 and channel 1 after configuring an appropriate phase mode.

```
@kernel
def run(self):
    self.core.reset()
    self.urukul0_cp1d.init()

    self.urukul0_ch0.init()
    self.urukul0_ch0.cfg_sw(True)
    self.urukul0_ch0.set_phase_mode(PHASE_MODE_TRACKING)
    self.urukul0_ch0.set_att(6.*dB)
    self.urukul0_ch1.init()
    self.urukul0_ch1.cfg_sw(True)
    self.urukul0_ch1.set_phase_mode(PHASE_MODE_TRACKING)
    self.urukul0_ch1.set_att(6.*dB)

    self.urukul0_ch0.set(frequency=10*MHz, phase=0.0)
    # 0.25 turns phase offset
    self.urukul0_ch1.set(frequency=10*MHz, phase=0.25)
```

Note that the phase difference between the 2 channels might not be exactly 0.25 turns, but it is a constant. It can be negated by adjusting the phase parameter.

Periodic RF pulse (AD9910 Only)

This example demonstrates that the RF signal can be modulated by amplitude using the RAM modulation feature of the AD9910. By default, RAM profiles are programmed to profile 0.

```

self.setattr_device("urukul0_ch1")

def prepare(self):
    self.amp = [0.0, 0.0, 0.0, 0.7, 0.0, 0.7, 0.7] # Reversed Order
    self.asf_ram = [0] * len(self.amp)

@kernel
def init_dds(self, dds):
    self.core.break_realtime()
    dds.init()
    dds.set_att(6.*dB)
    dds.cfg_sw(True)

@kernel
def configure_ram_mode(self, dds):
    self.core.break_realtime()
    dds.set_cfr1(ram_enable=0)
    self.urukul0_cpld.io_update.pulse_mu(8)
    self.urukul0_cpld.set_profile(0) # Enable the corresponding RAM profile
                                    # Profile 0 is the default
    dds.set_profile_ram(start=0, end=len(self.asf_ram)-1,
                        step=250, profile=0, mode=RAM_MODE_CONT_RAMPUP)
    self.urukul0_cpld.io_update.pulse_mu(8)
    dds.amplitude_to_ram(self.amp, self.asf_ram)
    dds.write_ram(self.asf_ram)

    self.core.break_realtime()
    dds.set(frequency=5*MHz, ram_destination=RAM_DEST_ASF)
    # Pass osk_enable=1 to set_cfr1() if it is not an amplitude RAM
    dds.set_cfr1(ram_enable=1, ram_destination=RAM_DEST_ASF)

    self.urukul0_cpld.io_update.pulse_mu(8)

@kernel
def run(self):
    self.core.reset()
    self.core.break_realtime()
    self.urukul0_cpld.init()

    self.init_dds(self.urukul0_ch0)
    self.configure_ram_mode(self.urukul0_ch0)

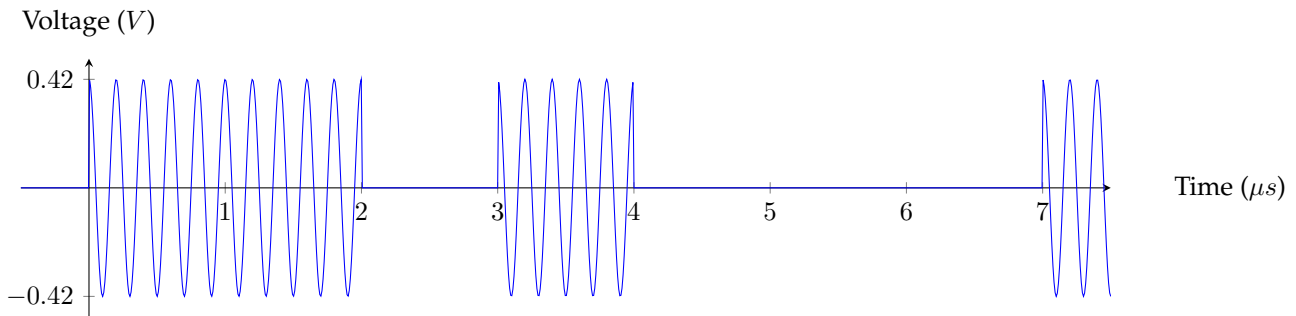
```

The generated RF output of the above example consists of the following features in sequence:

1. A 5 MHz RF pulse for 2 microseconds.
2. No signal for 1 microseconds.
3. A 5 MHz RF pulse for 1 microseconds.
4. No signal for 3 microseconds.

5. Go back to item 1.

The expected waveform is plotted on the following figure. Note that phase of the RF pulses may drift gradually. Urukul was operated with 50Ω termination for this waveform.

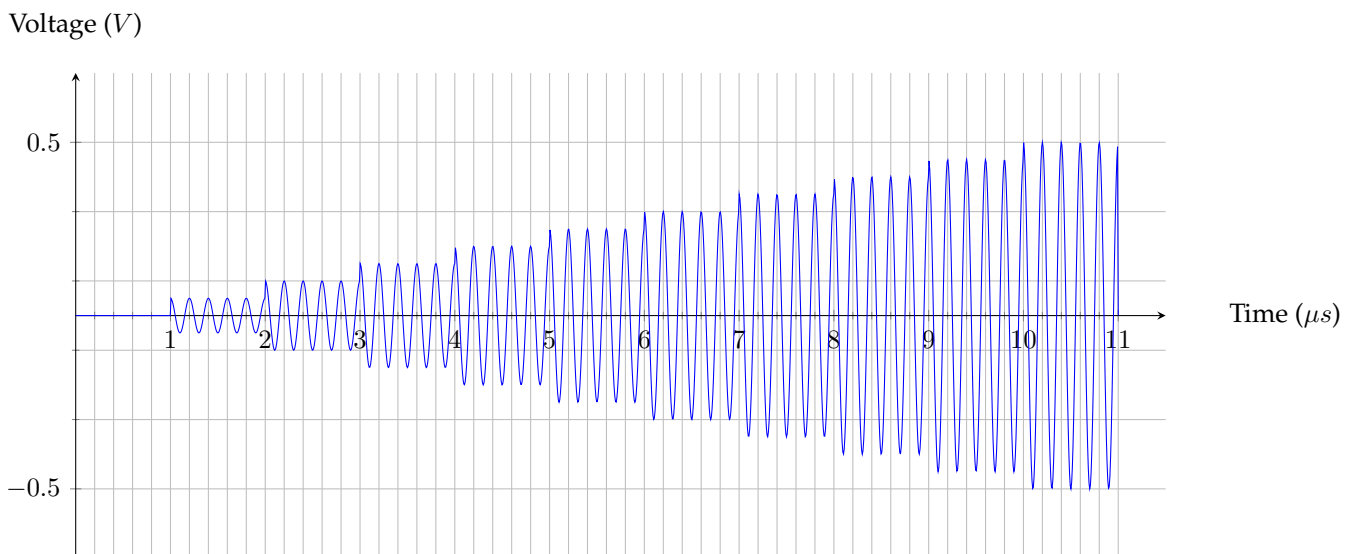


Simple amplitude ramp (AD9910 only)

An amplitude ramp of an RF signal can be generated by modifying the `self.amp` array in the previous example.

```
def prepare(self):
    # Reversed Order
    self.amp = [1.0, 0.9, 0.8, 0.7, 0.6, 0.5, 0.4, 0.3, 0.2, 0.1, 0.0]
    self.asf_ram = [0] * len(self.amp)
```

The generated RF output has an incrementing amplitude scale factor (ASF), increasing by 0.1 at every microsecond. Once the ASF reaches 1.0, it drops back to 0.0 at the next microsecond. The expected waveform over 1 cycle is plotted on the following figure. Note that phase of the RF pulses may drift gradually. Urukul was operated with 50Ω termination for this waveform.



RAM synchronization (AD9910 only)

Multiple RAM channels can also be synchronized. Similar to the 10 MHz single-tone RF signals, specify phase when calling `dds.set()` in `configure_ram_mode`. For example, set phase to 0 for the channels (`phase=0.0`):

```
dds.set(frequency=5*MHz, phase=0.0, ram_destination=RAM_DEST_ASF)
```

Then, replace the `run()` function with the following:

```
@kernel
def run(self):
    self.core.reset()
    self.core.break_realtime()
    self.urukul0_cpld.init()

    self.init_dds(self.urukul0_ch0)
    self.init_dds(self.urukul0_ch1)
    self.urukul0_ch0.set_phase_mode(PHASE_MODE_TRACKING)
    self.urukul0_ch1.set_phase_mode(PHASE_MODE_TRACKING)

    self.configure_ram_mode(self.urukul0_ch0)
    self.configure_ram_mode(self.urukul0_ch1)
```

Two phase-coherent RF signals with the same waveform as the previous figure (from either RAM examples) should be generated.

ARTIQ SU-Servo

ARTIQ also allows for the joint configuration of one or two 4410 DDS Urukul cards and a 5108 Sampler as an integrated servo for laser intensity stabilization and similar purposes. SU-Servo also supports other additional features, such as preconfigured profiles per channel and automatic integrator hold. Urukuls must be 4410 AD9910 variants (not 4412 AD9912) and set to SU-Servo mode.

SU-Servo System Description Entry

SU-Servo should be entered in the peripherals list of the corresponding core device in a single entry in the following format:

```
{
    "type": "suservo",
    "proto_rev": 9 // Urukul CPLD firmware version
    "sampler_ports": [0, 1],
    "urukul_ports": [[2, 3], [4, 5]], // second Urukul optional
    "clk_sel": 2, // select 0 to 2
    "synchronization": true, // or false
}
```

Enter the actual EEM port numbers used on the core device. Any ports can be used. SU-Servo may be configured with a single Urukul (using only half of the available Sampler channels) or with several; the `urukul_ports` field should be updated with a list of port pairs as appropriate.

For the `clk_sel` field, 0 represents the internal 100 MHz oscillator, 1 represents SMA input, and 2 represents MMCX input. To enable synchronization, the ARTIQ core device and Urukul should be clocked from the same source.

Example SU-Servo Code

In SU-Servo configuration, amplitude of the Urukul DDS output can be controlled with the Sampler ADC input through PI control, characterised by the following transfer function:

$$H(s) = k_p + \frac{k_i}{s + \frac{k_i}{g}}$$

In the following example, the DDS amplitude is set proportionally to the ADC input from Sampler. We initialize SU-Servo and all channels first. Note that the programmable gain of the Sampler is $10^0 = 1$ and the input range is [-10V, 10V].

```
@kernel
def run(self):
    self.core.reset()
    self.core.break_realtime()
    self.suservo.init()
    self.suservo.set_pgia_mu(0, 0) # unity gain
    self.suservo.cplds[0].set_att(0, 15.)
    self.suschannel0.set_y(profile=0, y=0.) # Clear integrator
```

Next, we set up the PI control as an IIR filter. It has -1 proportional gain k_p and no integrator gain k_i .

```
self.suschannel0.set_iir(
    profile=0,
    adc=0,          # take data from Sampler channel 0
    kp=-1.,         # -1 P gain
    ki=0./s,        # no integrator gain
    g=0.,           # no integrator gain limit
    delay=0.        # no IIR update delay after enabling
)
```

Then, configure the DDS frequency to 10 MHz with 3V input offset. When input voltage \geq offset voltage, the DDS output amplitude is 0.

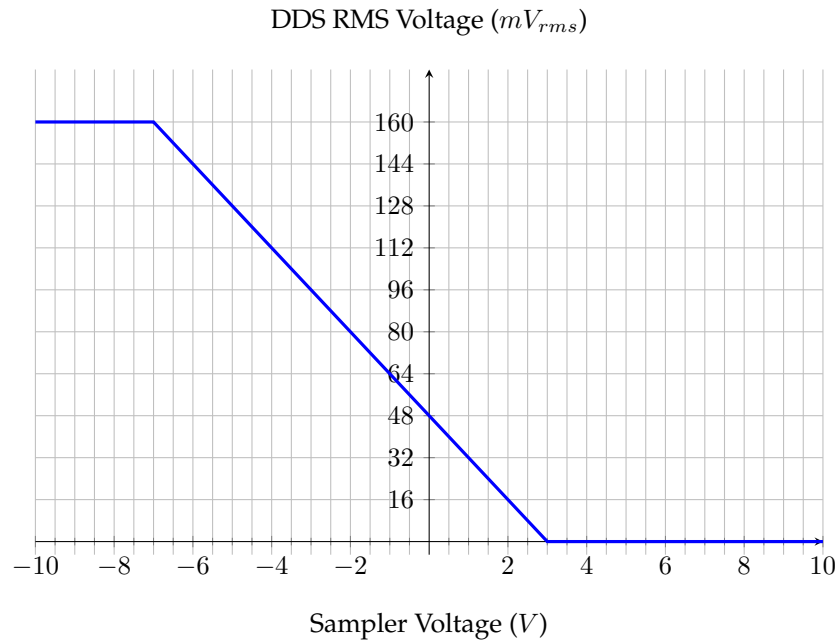
```
self.suschannel0.set_dds(
    profile=0,
    offset=-.3,     # 3 V with above PGIA settings
    frequency=10*MHz,
    phase=0.)
```

SU-Servo encodes the ADC voltage on a linear scale [-1, 1]. Therefore, 3V is converted to 0.3. Note that the ASF of all DDS channels is capped at 1.0 and the amplitude clips when ADC input $\leq -7V$ with the above IIR filter.

Finally, enable the SU-Servo channel with the IIR filter programmed beforehand:

```
self.suschannel0.set(en_out=1, en_iir=1, profile=0)
self.suservo.set_config(enable=1)
```

A 10 MHz DDS signal is generated from the example above, with amplitude controllable by ADC. The RMS voltage of the DDS channel against the ADC voltage is plotted. The DDS channel is terminated with 50Ω .



DDS signal should be attenuated. High output power affects the linearity due to the 1 dB compression point of the amplifier at 13 dBm output power. 15 dB attenuation at the digital attenuator was applied in this example.

Ordering Information

To order, please visit <https://m-labs.hk> and choose 4410/4412 DDS Urukul in the ARTIQ/Sinara hardware selection tool. Cards can be ordered as part of a fully-featured ARTIQ/Sinara crate or standalone through the 'Spare cards' option. Otherwise, orders can also be made by writing directly to <mailto:sales@m-labs.hk>.

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